



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,663	12/01/2003	Radoslav Danilak	NVID-P001159	5113
45594	7590	01/28/2008	EXAMINER	
NVIDIA C/O MURABITO, HAO & BARNES LLP			LEE, CHUN KUAN	
TWO NORTH MARKET STREET			ART UNIT	PAPER NUMBER
THIRD FLOOR			2181	
SAN JOSE, CA 95113				
MAIL DATE		DELIVERY MODE		
01/28/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/725,663	DANILAK ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Chun-Kuan (Mike) Lee	2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 31 October 2007.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.  
 4a) Of the above claim(s) 2-5,9-11,14-20 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,6-8,12 and 13 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 01 December 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | Paper No(s)/Mail Date: _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### **CONTINUED EXAMINATION UNDER 37 CFR 1.114**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/2007 has been entered.

### **RESPONSE TO ARGUMENTS**

2. Applicant's arguments with respect to claims 1, 6-8, 12 and 13 have been considered but are moot in view of the new ground(s) of rejection. Currently, claims 2-5 and 9-11 and 14-20 are withdrawn and claims 1, 6-8, 12 and 13 are pending for examination.

3. In response to applicant's arguments, on page 12, 2<sup>nd</sup> paragraph, regarding the amended independent claim 1 rejected under 35 U.S.C. 103(a) that Chisholm does not teach/suggest any memory mapped register or the use of such memory mapped register to transfer a disk I/O commands; applicant's arguments have fully been considered, but are not found to be persuasive.

Chisholm does teach/suggest that a memory mapped register (Fig. 3, ref. 203, 311) to be utilized for transferring of disk I/O commands (e.g. command blocks) (col. 5, l. 1 to col. 6, l. 8).

4. In response to applicant's arguments, on page 13, 3<sup>rd</sup> paragraph, regarding claim 6 rejected under 35 U.S.C. 103(a) that the combination of reference does not teach the CPB buffers are directed connected to the I/O engine for control in a manner independent of the arbiter; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that the features upon which applicant relies (i.e., the CPB buffers are directed connected to the I/O engine for control in a manner independent of the arbiter) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. In response to applicant's arguments, on page 13, last paragraph to page 14, 1<sup>st</sup> paragraph, regarding claim 7 rejected under 35 U.S.C. 103(a) that the combination of reference does not teach the chain memory are directly connected to the I/O engine for control in a manner independent of the arbiter; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that the features upon which applicant relies (i.e., the chain memory are directly connected to the I/O engine for control in a manner independent of the

arbiter) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

## I. REJECTIONS BASED ON PRIOR ART

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 6-8, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chisholm et al. (US Patent 5,968,143) in view of Wood et al. (US Patent 6,915,363), Davis et al. (US Patent 6,298,407) and Winkler et al. (US Pub. 2004/0024948).

7. As per claims 1 and 8, Chisholm teaches a bridge component for implementing efficient disk I/O for a computer system, comprising:

a bus interface (Fig. 3, ref. 109, 111) for interfacing with a processor (Fig. 1, ref. 103) and a system memory (Fig. 3, ref. 301) of the computer system;  
a disk controller (Fig. 3, ref. 201, 203, 209, 213) for executing disk transactions for the computer system, the disk controller further comprising:  
a disk I/O engine (Fig. 3, ref. 209) coupled to the bus interface;

a bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine, wherein the bypass register as memory mapped (col. 5, l. 1 to col. 6, l. 8); and a device interface (Fig. 3, ref. 213) coupled to the disk I/O engine (Fig. 3, ref. 209) for interfacing the disk I/O engine with a disk drive (e.g. SCSI RAID disk drives) (Fig. 1, ref. 114 and col. 4, ll. 26-36), the disk I/O engine further configured to execute a disk transaction by processing the disk transaction information from the memory mapped bypass register (Fig. 3, ref. 203, 311) coupled to the disk I/O engine (col. 5, l. 1 to col. 6, l. 8), as the command/data blocks are transferred to the memory mapped bypass register for implementing disk transaction and bypass the writing of a set of 8 bit registers in the disk controller as implemented in ATA disk drives.

Chisholm does not teach the bridge component comprising a bus master controller ...; an arbiter coupled to the bus master controller ...; and wherein the disk I/O engine is configured to cause a start up of the disk drive upon receiving a disk start up command from the processor, the start up command configured to hide a start latency of the disk drive.

Wood teaches a system and a method comprising a host computer (Fig. 3, ref. 302); an array of disk drives (Fig. 3, ref. 318) comprising a redundant array of Inexpensive discs (RAID) (col. 1, ll. 47-51); transferring a start command to the array of disk drives via a subsystem controller (Fig. 3, ref. 314) to cause the array of disk drives to start up, as the timing for

transferring the start command to each disk drive is controlled and regulated (col. 3, II. 10-27 and col. 6, II. 1-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Wood's start command into Chisholm's bridge component for the benefit of enabling proper start up of the array of disk drives utilizing out-of-band signaling without exceeding the capability of the power supply (Wood, col. 1, II. 52-60 and col. 3, II. 1-9) to obtain the invention as specified in claims 1 and 8. The resulting combination of the references further teaches the bridge component comprising wherein the subsystem controller (e.g. disk I/O engine) is configured to cause the disk drive to start up as the start command (e.g. disk start up command) is received from the host computer (e.g. processor).

Chisholm and Wood do not teach the bridge component comprising a bus master controller ...; an arbiter coupled to the bus master controller ...; and wherein the start up is configured to hide a start latency of the disk drive.

Davis teaches a bridge component comprising a number of data queues implemented to hide the delay associated with the requesting and obtaining access to a bus coupled to a corresponding peripheral as data can be transferred without delay (col. 1, I. 61 to col. 2, I. 3).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Davis's data queues into Chisholm and Wood's bridge component for the benefit of synchronizing the transferring of data between the initiator

and the target (Davis, col. 2, ll. 10-13) to obtain the invention as specified in claims 1 and 8. The resulting combination of the references further teaches the bridge component comprising wherein the subsystem controller (e.g. disk I/O engine) is configured to cause the disk drive to start up as the start command (e.g. disk start up command) is received from the host computer (e.g. processor), wherein the start command would be configured to hide the delay associated with the disk drive's start latency, as data to be transferred can be send following the transferring of the start command with delay.

Chisholm, Wood and Davis do not expressly teach the bridge component comprising a bus master controller ...; and an arbiter coupled to the bus master controller ....

Winkler teaches a system and a method comprising:  
a bus master controller coupled to a disk I/O engine (e.g. hard disk controller) [0013]; and  
an arbiter coupled to the bus master controller and the disk I/O engine (e.g. hard disk controller), to coordinate data transfers within the disk controller [0013], wherein the inclusion of the arbitration function into the disk controller would enable proper coordination of the data transferring for disk drive system such as RAID.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Winkler's bus master controller and arbitration into Chisholm, Wood and Davis's disk controller for the benefit of increasing the operation

speed, as well as improving reliability and the efficiency in the transferring of data (Winkler, [0017]) to obtain the invention as specified in claims 1 and 8.

8. As per claims 6 and 12, Chisholm, Wood, Davis and Winkler teach all the limitations of claims 1 and 8 as discussed above, where Chisholm further teaches the bridge component wherein the disk controller further comprising a CPB pointer buffer (Chisholm, command address queue 309 of Fig. 3) coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers (e.g. addresses pointing to where the command block are stored) to extend to a number of disk transactions scheduled for execution by the disk I/O engine (Chisholm, col. 5, l. 1 to col. 6, l. 8).

9. As per claims 7 and 13, Chisholm, Wood, Davis and Winkler teach all the limitations of claims 1 and 8 as discussed above, where Chisholm teaches the bridge component wherein the disk controller further comprising a chain memory (Chisholm, Fig. 3, ref. 309, wherein the addresses are subsequently stored and retrieved in a chain) coupled to the disk I/O engine for buffering a plurality of CPBs (Chisholm, Fig. 3, ref. 304) to extend to a number of disk transactions scheduled for execution by the disk I/O engine (Chisholm, col. 5, l. 59 to col. 6, l. 8).

## **II. CLOSING COMMENTS**

### **Conclusion**

#### **a. STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

#### **a(1) CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1, 6-8, 12 and 13 have received a first action on the merits and are subject of a first action non-final.

#### **b. DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

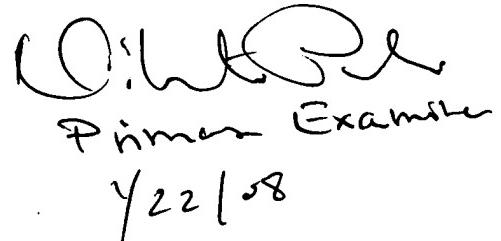
### **IMPORTANT NOTE**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 08, 2008

Chun-Kuan (Mike) Lee  
Examiner  
Art Unit 2181

  
Primary Examiner  
1/22/08